Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device having a self-aligned contact, the semiconductor device comprising:

a plurality of conductive patterns formed to be adjacent to one another by sequentially stacking and patterning a first conductive layer and a mask layer on a particular underlying layer;

a first insulation layer filling a gap between adjacent conductive patterns, the first insulation layer being formed of a first insulating material and being formed laterally adjacent to and not underneath the conductive patterns;

a second insulation layer having a spacer shape, the second insulation layer formed at the sides of each conductive pattern and over the first insulation layer, the second insulation layer being formed of a second insulating material different from the first insulating material; and

a second conductive layer filling a contact hole which is self-aligned with respect to the second insulation layer between adjacent conductive patterns, the contact hole passing through the first insulation layer, the first insulation layer extending between adjacent conductive patterns and between the second conductive layer and the conductive patterns and having a planar top surface throughout the entire distance between ~~adjacent~~ at least one of the conductive patterns and the second conductive layer.

2. (Original) The semiconductor device of claim 1, wherein the top of the first insulation layer is lower than the top of the first conductive layer of each conductive layer pattern.

3. (Original) The semiconductor device of claim 1, wherein the top of the first insulation layer is higher than the top of the first conductive layer of each conductive layer pattern.

4. (Original) The semiconductor device of claim 1, wherein an etching rate of the first insulation layer is larger than that of the second insulation layer.

5. (Original) The semiconductor device of claim 1, wherein the dielectric constant of the first insulation layer is smaller than that of the second insulation layer.

6. (Original) The semiconductor device of claim 1, wherein the first insulation layer is formed of a silicon oxide layer.

7. (Original) The semiconductor device of claim 1, wherein the second insulation layer is formed of a silicon nitride layer.

8. (Original) The semiconductor device of claim 1, further comprising a third insulation layer provided between the first insulation layer and the sides of each conductive layer pattern and between the second insulation layer and the side of the conductive layer pattern.

9. (Original) The semiconductor device of claim 8, wherein the third insulation layer is formed of a silicon nitride layer to a thickness of 50-200 Å.

10. (Original) The semiconductor device of claim 1, further comprising a fourth insulation layer provided on the surface of the underlying layer except for a portion contacting the second conductive layer and on the surfaces of the conductive layer patterns.

11. (Original) The semiconductor device of claim 10, wherein the fourth insulation layer is formed of a silicon nitride layer to a thickness of 50-200 Å.

12. (Canceled)

13. (Canceled)

14. (Original) The semiconductor device of claim 1, wherein the first conductive layer of each conductive layer pattern is a bit line, and the second conductive layer serves to connect a storage electrode of a semiconductor capacitor to a semiconductor substrate.

15. (Original) The semiconductor device of claim 1, wherein the first conductive layer of each conductive layer pattern is a gate electrode, and the contact contacts the surface of a semiconductor substrate.

16. (Withdrawn)

17. (Withdrawn)

18. (Withdrawn)

19. (Withdrawn)

20. (Withdrawn)